


Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office		Docket No. D5116-00002		Serial No. 09/675,427	
INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION (Use several sheets if necessary)		Applicant Saxena et al.			
		Filing Date September 29, 2000		Group Art Unit 2812	



U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
H.D.	AA	5,767,542	6/16/98	Nakamura	57	296	
H.D.	AB	5,773,315	6/30/98	Jarvis	438	14	
H.D.	AC	6,184,048	2/6/01	Ramon	438	14	

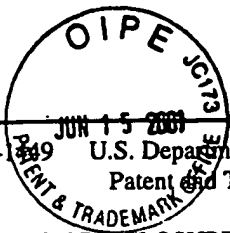
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FOREIGN PATENT DOCUMENTS							
DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
					YES	NO	
						X	
						X	

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)		
H.D.	A	International Search Report dated 09 APR 2001
H.D.	B	Khare et al., "Extraction of Defect Characteristics for Yield Estimation Using The Double Bridge Test Structure", IEEE, May 1991, pages 428-432
H.D.	C	Yun et al., "Evaluating the Manufacturability of GaAs/AlGaAs Multiple Quantum Well Avalanche Photodiodes Using Neural Networks, IEEE, Oct 1997, pages 105-112
H.D.	D	Hansen et al., "Effectiveness of Yield-Estimation and Reliability-Prediction Based on Wafer Test-Chip Measurements", IEEE, Jan 1997, pages 142-148

EXAMINER <i>Hong-der Day</i>	DATE CONSIDERED 3/24/05
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.



Form PTO-449 INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION (Use several sheets if necessary)	Docket No. D5116-00002	Serial No. 09/675,427
	Applicant Saxena et al	
	Filing Date Sept. 29, 2000	Group Art Unit 2812

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
H.D.	A	3,751,647	8/7/73	Maeder et al.	235	151.11	
H.D.	B	5,822,258	10/13/98	Casper	365	201	
H.D.	C	5,852,581	12/22/98	Beffa et al	365	201	

FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)		
H.D.	D	Khare et al., "Yield Oriented Computer-Aided Defect Diagnosis", IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No. 02, May 1995 (02.05.1995), pages 195-206
H.D.	E	International Search Report dated 08 JUN 2001

EXAMINER	<i>Henry Lee Day</i>	DATE CONSIDERED	3/24/05
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Form PTO-1449 U.S. Department of Commerce
Patent and Trademark OfficeDocket No.
D5116-00002Serial No.
09/675,427INFORMATION DISCLOSURE STATEMENT
IN AN APPLICATIONApplicant
Saxena et al.Filing Date
November 29, 2000Group Art Unit
2812

Use several sheets if necessary)

U.S. PATENT DOCUMENTS

INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
H.D.	A	4,835,466	5/30/89	Maly et al.	324	158R	

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OCT 12 2001
Technology Center 2100

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

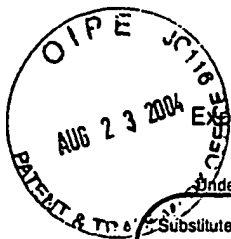
OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

H.D.	B	Nurani et al., "In-Line Yield Prediction Methodologies Using Patterned Wafer Inspection Information", IEEE Transactions on Semiconductor Manufacturing, Vol. 11, No. 1, Feb 1998, pp.40-47						

EXAMINER

DATE CONSIDERED 3/24/05

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Application Number	09/675,427
Filing Date	September 29, 2000 AUG 27 2004
First Named Inventor	Sharad Saxena Technology Center 2100
Art Unit	2128
Examiner Name	Morella I Rosales Hanner
Attorney Docket Number	D5116-00002

Sheet 1 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
H.D.		Y. CHENG et al., "MOSFET Modeling and BSIM User Guide." Kluwer Academic Publishers, Boston, 1999	✓
H.D.		CONTI et al. "Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect." IEEE Transactions on Computer-Aided Design, Vol. 18, pp. 582-596, May 1999	
H.D.		GUARDIANI et al., "Applying a submicron mismatch model to practical IC design." IEEE Custom Integrated Circuits Conference, San Diego (CA), May 1994	
H.D.		HUIJSING et al., "Low-Power Low-Voltage VLSI Operational Amplifier Cells." IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 42, No. 11, pp. 841-852, November 1995	
H.D.		HWANG, et al., "Universal Constant-gm Input-Stage Architectures for Low-Voltage Op Amps." IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 42, No. 11, pp. 886-894, November 1995.	
H.D.		PINEDA DE GYVEZ et al., "Integrated Circuits Manufacturability: the Art of Process and Design Integration." pp. 158-166, IEEE Press, New York, 1999	
H.D.		FELT et al., "Hierarchical Statistical Characterization of Mixed-Signal Circuits Using Behavioral Modeling." IEEE-ACM International Conference on Computer Aided Design, San Jose (CA), November 1996	
H.D.		MICHAEL et al., "Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits." Kluwer Academic Publishers, Boston, 1993	
H.D.		MICHAEL et al., "Statistical Modeling of Device Mismatch for Analog Integrated Circuits." IEEE Journal of Solid-State Circuits, Vol. 27, No. 2, February 1992	
H.D.		"pdPCA User's Manual." Version 7, PDF Solutions, Inc., San Jose, 1998	

Examiner Signature	<i>Homer A. Day</i>	Date Considered	3/24/05
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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